What is claimed is:

1. A semiconductor device comprising:

a first semiconductor layer of a first conductivity type;

a second semiconductor layer of a second conductivity type formed on the first semiconductor layer, the second conductivity type being different from the first conductivity type;

a third semiconductor layer of the first conductivity type selectively formed on the second semiconductor layer;

a trench formed through the third semiconductor layer and the second semiconductor layer to reach the first semiconductor layer;

a gate dielectric film formed along side and bottom surfaces of the trench; and

a gate electrode formed to be in contact with the gate dielectric film at the side surfaces of the trench, surfaces of the gate electrode that are opposite to the surfaces contacting the gate dielectric film, and the gate dielectric film at a bottom of the trench forming a hollow portion extending from the bottom to an opening side of the trench.

2. The semiconductor device according to claim 1, wherein the gate electrode includes a first electrode layer formed of a first electrode material, the first electrode layer being in contact with the gate dielectric film, and a second electrode layer formed of a second electrode material, the second electrode layer being in contact with the first electrode layer.

3. The semiconductor device according to claim 2, wherein a resistance of the second electrode material is lower than that of the first electrode material.

4. The semiconductor device according to claim 2, wherein the second electrode material is a silicide.

5. The semiconductor device according to claim 3, wherein the second electrode layer is formed of a silicide, and thicker than the first electrode layer.

6. The semiconductor device according to claim 1, wherein the gate electrode is formed of a silicide.

7. The semiconductor device according to claim 1, further comprising a fourth semiconductor layer of the first conductivity type formed to be in contact with a surface of the first semiconductor layer opposite from the second semiconductor layer, a concentration in the fourth semiconductor layer being higher than that in the first semiconductor layer.

8. The semiconductor device according to claim 7, wherein a plurality of the third semiconductor layers are formed on the second semiconductor layer, a plurality of the trenches are formed each corresponding to one of the third semiconductor layers, the gate dielectric film and the gate electrode are formed in each trench, and the gate electrodes in the trenches are commonly connected electrically.

9. The semiconductor device according to claim 8, further comprising a dielectric film covering an upper surface of the gate electrode of each trench, and a source electrode covering the dielectric film and being electrically connected to the third semiconductor layers.

10. The semiconductor device according to claim 9, further comprising a fifth semiconductor layer of the second conductivity type formed in the second semiconductor layer, a concentration in the fifth semiconductor layer being higher than that in the second semiconductor layer.

11. The semiconductor device according to claim 10, wherein the source electrode is electrically connected to the fifth semiconductor layer.

12. The semiconductor device according to claim 9, further comprising a drain electrode formed to be in contact with a surface of the fourth semiconductor layer opposite from the first semiconductor layer, the drain electrode being electrically connected to the fourth semiconductor layer.

13. The semiconductor device according to claim 8, wherein the gate electrode includes a first electrode layer formed of a first electrode material, the first electrode layer being in contact with the gate dielectric film, and a second electrode layer formed of a second electrode material, the second electrode layer being in contact with the first electrode layer.

14. The semiconductor device according to claim 13, wherein a resistance of the second electrode material is lower than that of the first electrode material.

15. The semiconductor device according to claim 13, wherein the second electrode material is a silicide.

16. The semiconductor device according to claim 14, wherein the second electrode layer is formed of a silicide, and thicker than the first electrode layer.

17. The semiconductor device according to claim 8, wherein the gate electrode is formed of a silicide.

18. A method of manufacturing a semiconductor device comprising a semiconductor substrate, the semiconductor substrate including a first semiconductor layer of a first conductivity type, a second semiconductor layer of a second conductivity type formed on the first semiconductor layer, the second conductivity type being different from the first conductivity type, and a third semiconductor layer of the first conductivity type selectively formed on the second semiconductor layer, forming a trench through the third semiconductor layer and the second semiconductor layer to reach the first semiconductor layer;

the method comprising:

forming a gate dielectric film along side and bottom surfaces of the trench;

forming a first electrode layer of polycrystalline silicon along the gate dielectric film in the trench;

removing the first electrode layer at a bottom of the trench to

leave the first electrode layer at the side surfaces;

forming a high melting-point metal layer covering the first electrode layer remaining on the side surfaces of the trench;

performing a heat treatment to allow silicon of the first electrode layer and the high melting-point metal to react with each other to form a first high melting-point metal silicide layer; and

removing unreacted high melting-point metal to form a hollow portion extending from the bottom to an opening side of the trench with the gate dielectric film at the bottom of the trench and surfaces of the first high melting-point metal silicide layer.

19. The method of manufacturing a semiconductor device according to claim 18, wherein in the forming of the first high melting-point metal silicide layer, the first electrode layer is fully silicided.

20. The method of manufacturing a semiconductor device according to claim 18, further comprising:

forming a second electrode layer of polycrystalline silicon along the first high melting-point metal silicide layer in the trench;

removing the second electrode layer at the bottom of the trench to leave the second electrode layer at the side surfaces;

forming a high melting-point metal layer covering the second electrode layer remaining on the side surfaces of the trench;

performing a heat treatment to allow silicon of the second electrode layer and the high melting-point metal to react with each other to change all of the second electrode layer on the side surfaces of the trench to a second high melting-point metal silicide layer; and

removing unreacted high melting-point metal to form a hollow portion extending from the bottom to the opening side of the trench with the gate dielectric film at the bottom of the trench and surfaces of the second high melting-point metal silicide layer.